# Atharva Shah

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https://atharvashah.org/

## OBJECTIVE

Seeking opportunities in RF Systems/RFIC + Mixed Signal IC. Prior background in Digital Modems, FPGAs, and analog design.

## EDUCATION

**University of California, San Diego** **GPA: 3.913**
**MS Electrical Engineering**, RFIC + Mixed Signal IC Jun. 2025
**BS Electrical Engineering**, Circuits/Systems, Digital Signal Processing Dec. 2023

## WORK EXPERIENCE

**ASIC / MMIC Design Intern** Jun 2024 - Sep 2024
Keysight Technologies – Research and Development Colorado Springs, CO

- Upcoming – During Summer of 2024

**Electrical Engineering Intern** Jun 2022-Aug 2022
West Coast Solutions Huntington Beach, CA

- Designed and laid out **100Ω diff-pair stripline** board for testing of Cameralink data.
- Developed **telemetry and power circuits** for a Turbo-Brayton cryocooler to be used in a NASA program.
- Designed a **power supply** circuit to distribute power for **op-amps, muxes, ADCs,** and **FPGA** core
- Tested inrush current and noise of a PSU with an **oscilloscope**

**Electrical Engineering Intern** Jun 2023-Sep 2023
Lockheed Martin – Space Sunnyvale, CA

- Designed heater control and restraint release **FET drivers** and boards for use on a satellite platform.
- Implemented algorithms in **Simulink** which were then transpiled to HDL using **HDL Coder**
- Designed an architecture for direct-write testing of LSRAM inside a **PolarFire FPGA** using Libero suite.
- Pipelined both SystemVerilog and Simulink designs in order to meet post-pnr timing requirements.

## PROJECTS

**Fully Integrated 3-Level Buck Converter (PMICs)** (gpdk 45nm)

- System and Transistor level design of a fully integrated 3-level buck converter at $f_s$=40MHz, $\eta$ =0.91
- Analog blocks include: Error OTAs, Comparators, OpAmps, PWM generation
- Digital blocks include: cascoded level shifters, gate drivers, deadtime control

**Two-Stage Folded Cascode Op-Amp** (IBM 180nm)

- Sized a Two-Stage Folded Cascode Op-Amp in order to meet >65dB DC gain, and >60MHz UGBW constraints.
- Sized high-swing bias and gm-reference generation to provide accurate current biasing to the circuit

**Digital Modem Design**

- Implemented a **fully Digital OFDM modem + demodem** including cyclic prefix and **equalization**.
- Created digital **Phase Lock Loop (PLL)** and **Timing Recovery** implementations in MATLAB.
- Developed programs for QPSK equalization, I-Q balancing, and DC cancellation in MATLAB

**8-bit Adder Transistor Level Design** (gpdk 45nm)

- Designed an 8-bit Ladner-Fischer adder using **Cadence Virtuoso** in 45nm
- Utilized odd-even PG network and increased critical path sizing to optimize design from 1.8GHz to 4.3GHz
- **Layout** of the following digital design components: NAND, NOR, INV, Ring Oscillator

**Butler HTTP Server** - https://github.com/Shah06/butler

- Wrote a **multithreaded web server** in Java, with NodeJS-esque syntax

## TECHNICAL SKILLS (Keyword soup)

**Equipment** - Arbitrary Waveform Generator (AWG), BER Tester, Oscilloscope, VNA, Spectrum Analyzer, Function Generator, Keysight M8190A AWG, Keysight M8046A BERT
**Languages** - C, MATLAB, Simulink, Python, Verilog/SystemVerilog, C++, Java, ARM
**Software** - Cadence Virtuoso, Keysight ADS, Allegro, LTSpice, FPGA (Vivado, Libero, Quartus, ModelSim)